IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Luiz A. BARROSO	§ §	Anticipated Group Art Unit:	2187
Serial No.:	09/878,984	§ §	Anticipated	
Filed:	June 11, 2001	§ §	Examiner:	K. Takeguchi
For:	Multiprocessor Cache Coherence System And Method In Which Processor Nodes And Input/ Output Nodes Are Equal Participants	§ § § § § § § § §	Docket No.:	200302253-2

PRELIMINARY AMENDMENT

Mail Stop Patent Application
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Date: October 31, 2003

Sir:

The Examiner is respectfully requested to enter the following amendment prior to the calculation of fees and the initial examination of the present above-identified continuation patent application under 1.53(b) in which the parent case Serial No. 09/878,984 survives.

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 4 of this paper.

Remarks/Arguments begin on page 8 of this paper.